UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/430,350	10/29/1999	MASSIMO SUTERA	P4158/PJM	7163

32291 7590 01/08/2004

MARTINE & PENILLA, LLP
710 LAKEWAY DRIVE
SUITE 170
SUNNYVALE, CA 94085

EXAMINER	
JONES, HUGH M	
ART UNIT	PAPER NUMBER
2128	18

DATE MAILED: 01/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/430,350	SUTERA ET AL.	
	Examiner	Art Unit	
	Hugh Jones	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on 24 November 2003.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-8,14-17,25,27-30,36-39 and 47 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-8, 14-17, 25, 27-30, 36-39, 47 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-8, 14-17, 25, 27-30, 36-39, 47 of U.S. Application 09/430,350 are pending.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1-2, 5-8, 14-15, 27-30, 36-37 are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for "modifying the net to reduce the length by inserting a buffer", does not reasonably provide enablement for a broader teaching of modifying the net. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the invention commensurate in scope with these claims.

Claim Interpretations

4. The Examiner has given the claims their broadest reasonable interpretation.

5. The following disclosures from the specification are interpreted as *Applicant's Admission regarding prior art*:

- page 2 (first paragraph) is Applicant's Admission regarding prior art teaching of the relationship between drivers and noise and the use of different drivers to counteract the effects of noise;

- figures 1-2 (and second full paragraph, page 5, specification, relating to figure 2);

- page 3, last paragraph, is Applicant's admittance regarding the ability of a skilled artisan;

- page 5, (first full paragraph) is Applicant's Admission regarding prior art teaching of curves for various driver circuits of noise amplitude vs. length of lines;

- page 5, (first full paragraph) is Applicant's Admission regarding prior art teaching of the lower susceptibility of wires to noise for stronger drivers;

- page 6, (second paragraph - lines 1-4) is Applicant's Admission regarding prior art teaching of criterion for noise levels.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-8, 14, 16-19, 25-30, 36, 38-41, 47-48 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by *Petschauer et al.*.

8. ***Petschauer et al. ('506)*** disclose "*Method of fabricating IC chips with equation estimated peak crosstalk voltages being less than noise margin.*" They further disclose that in one method according to the present invention, an integrated circuit chip is fabricated by the following steps:

1) providing a trial layout in the chip for a victim net and a set of aggressor nets which have segments that lie next to the victim net;

2) assigning to the trial layout of the victim net, the parameters of--a line capacitance, a line resistance, and a driver output resistance; and assigning to the trial layout of each aggressor net, the parameters of--a coupling capacitance to the victim net, and a voltage transition;

3) estimating, for each aggressor net, a respective peak crosstalk voltage V.sub.p which the aggressor net couples into the victim net as a function V.sub.p =K(e.sup.-X -e.sup.-Y) where K, X, and Y are products of said parameters;

4) modifying said trial layout and repeating the assigning and estimating steps until a summation of the estimated peak crosstalk voltages in the victim net is within an acceptable level; and,

5) building the chip with the modified layout for which the summation is within the acceptable level. See fig. 4-9, 25 and corresponding text.

9. **Claims 1-8, 14-17, 25, 27-30, 36-39, 47 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Li et al. (A repeater optimization methodology for deep sub-micron high-performance processors. - 1997).**

10. **Li et al.** disclose that as process technology scales down to deep sub-micron and the frequency of a high-performance processor increases beyond 300 MHz, coupling induced signal integrity problems become more severe. Ignoring coupling effects can lead to functional failures or speed degradation. As a result, the traditional approach of **repeater** insertion driven by propagation **delay** and slew rate optimization becomes inadequate. The authors propose a design methodology to select optimal **repeaters** for high-performance processors by considering not only the **delay** and slew rate, but also **crosstalk** effects. A concurrent decision diagram (CDD) is further suggested to achieve **crosstalk** constraints with various trade-offs. See section IV (Proposed Methodology) including step 1 (Delay-ratio consideration); step 2 (Repeater-delay consideration); step 4 (With vs. witout repeaters: delay and skew); step 5 (Crosstalk consideration); step 6 (CDD alternatives and trade-offs). Particularly note fig. 3 (crosstalk voltage dependence on wire length); fig. 6 (design algorithm taking into consideration delay, crosstalk wire length, driver strength in an iterative constraint methodology); fig. 11 (delay dependence on presence of repeaters and as a function of wire length); fig. 13-14 (relationship between crosstalk and driver strength); fig. 15 (relationship between crosstalk, wire length and driver strength).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the**

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. The factual inquiries set forth in *Graham v. John Deere Co.*, 148 USPQ 459, that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or unobviousness.

13. Claims 1-8, 14, 16-17, 25, 27-30, 36, 38-39, 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over [Alpert et al. (6,117,182) or Tawada or Jones et al. or Dwyer et al.] in view of (Applicant's Own Admission) or Oh et al. or Davis et al. or Yang et al. or Petschauer et al. or Li et al..

- Alpert et al. ('182) disclose a method for ***optimal insertion of buffers into an integrated circuit design***. A model representative of a plurality of circuits is created where each circuit has a receiving node coupled to a conductor and a source. A receiving node is selected from the modeled plurality of circuits and circuit noise is calculated for the selected receiving node utilizing the circuit model. ***If the calculated circuit noise exceeds an acceptable value an optimum distance is computed from the receiving node on the conductor for buffer insertion. See "noise slack"*** at col. 11, for example as it relates to the recited "curves". In a multi-sink circuit merging of the noise calculation for the two receiving circuits must be accomplished. ***If an***

intersection of conductors exists between the receiving node and the optimum distance a set of candidate buffer locations is generated. The method then prunes inferior solutions to provide an optimal insertion of buffers. See fig. 3-6. See entire disclosure.

- **Tawada** discloses a system for automatically improving and removing the crosstalk error for reducing the number of designing steps, the switching timing of each net is detected from the results of path delay analysis and crosstalk analysis is carried out so as to take account of the overlap of the switching timing between a net under inspection and a neighboring net. A delay gate insertion unit inserts a delay gate to a neighboring net having timing overlap with the net under inspection undergoing crosstalk error as detected or a net on a path to which belongs the neighboring net. The delay gate inserted is such a delay gate as can improve the crosstalk and as does not produce path delay error. The delay gate inserted by the delay gate placing unit is placed on the route of the net at such a position as can improve the crosstalk error of the net under inspection. An incremental wiring unit re-wires a net divided by the insertion and placing of the delay gate and a net affected by the insertion and placing of the delay gate to improve the crosstalk error automatically. See fig. 1, 4-5, 9, 14-19 and corresponding text.

- **Jones et al**. disclose ***automated cost-based placement*** (wherein ***cost*** includes timing and ***noise***) of library cells (including buffers) and the use of Design Rule checking (DRC). See: abstract; fig. 1-3, fig. 4 (cell library and speed paths), fig. 5 (timing); col. 1-2 (general background); col. 3, lines 29-65 (details about the placement,

cost function, cell library, speed, ***noise***); col. 5, lines 47-60 (cell library, buffers); col. 6, lines 36-47 (goals of optimized placement); col. 7, lines 3-43 (cost and iteration); col. 8, lines 9-42 (***goals of optimized placement***); col. 9-10 (automated, iterative, cost-based layout; timing, ***noise***; DRC). ***Jones et al. teaches noise avoidance as one of many criteria for optimal cell placement.***

- Dwyer et al. disclose a method (and a system for using the method) for ***placing a semiconductor circuit device between a driver and one or more receivers on the floor space of a chip***. The method includes the steps of: determining respective distances between the driver and each of the one or more receivers; determining a shortest of the distances; determining midpoint along the shortest distance; determining whether the midpoint is predesignated to the floor space of one or more blocking semiconductor circuit devices; ***placing the repeater at the midpoint if the midpoint is not predesignated to the one or more blocking semiconductor circuit devices; and applying a backoff algorithm to incrementally back away from the midpoint to an optimal location, and placing the repeater at the optimal location, if the midpoint is predesignated to the one or more blocking semiconductor circuit devices.*** The method can also include the steps of: determining whether the to be placed semiconductor circuit device can be placed at a set of incremental locations located along one or more axes away from the midpoint; and placing the to be placed semiconductor circuit device at one of the one or more acceptable incremental locations. The step of determining the set of incremental locations can be performed in a spiral pattern away from the midpoint. ***The***

semiconductor circuit device to be placed can be, for example, a repeater along the path of a net (length of wire) to regenerate a propagated signal.

14. (Alpert et al. or Tawada or Jones et al. or Dwyer et al.) teach the limitations as discussed but do not disclose that the curves define a relationship between conductor length and noise and further do not disclose replacement of drivers.

15. Applicants have admitted the following:

- page 2 (first paragraph) is Applicant's Admission regarding prior art teaching of the relationship between drivers and noise and the use of different drivers to counteract the effects of noise;
- figures 1-2 (and second full paragraph, page 5, specification, relating to figure 2);
- page 3, last paragraph, page 9, last paragraph and page 10 are Applicant's admittance regarding the ability of a skilled artisan;
- page 5, (first full paragraph) is Applicant's Admission regarding prior art teaching of curves for various driver circuits of noise amplitude vs. length of lines;
- page 5, (first full paragraph) is Applicant's Admission regarding prior art teaching of the lower susceptibility of wires to noise for stronger drivers;
- page 6, (second paragraph - lines 1-4) is Applicant's Admission regarding prior art teaching of criterion for noise levels.

16. Oh et al. disclose "*A scaling scheme and optimization methodology for deep sub-micron interconnect.*" They further disclose the requirements for interconnect in deep-submicron technologies and identify critical factors that will require innovations in

process technology, process integration and circuit-and-system design techniques. They also describe a scaling scheme for global lines to optimize the interconnect for a given application domain such as microprocessors, ASIC's or memory. For local interconnect they demonstrate that cross-talk is the major challenge which can be addressed by selectively using larger drivers to reduce cross-talk noise when necessary. An interconnect system optimization methodology is also presented that can be used to determine the geometry parameters of a multi-level interconnect system based on the criterion for performance and reliability. See pp. 321-322, fig. 2-4, 13-14.

17. ***Davis et al.*** disclose "*Length, scaling, and material dependence of crosstalk between distributed RC interconnects.*" They further disclose that new general expressions for the transient response time and peak crosstalk of coupled distributed RC interconnects driven by a voltage source with finite rise-time and source impedance are presented. New compact expressions for peak crosstalk voltage reveal a previously unrecognized strong dependence of crosstalk on interconnect length, scaling, driver impedance, and materials properties for typical rise-time dominant interconnect circuits. See pg. 228, fig. 3-5.

18. ***Yang et al.*** disclose "*Deep submicron on-chip crosstalk [and ANN prediction]*". They further disclose the effect of crosstalk using three deep submicron technologies. They start the experiment by comparing the different technologies. Then they concentrate on 0.18 /spl mu/m technology to examine the effect of different parameters on the crosstalk voltage peak and circuit timing. The parameters of interest are the size of the driving and load device and the length of the coupled line. The results confirmed

that finer technologies cause higher impact. The magnitude of crosstalk in 0.18 /spl mu/m may be high enough to violate noise margin. Preliminary layout guidelines are deduced. To facilitate applying them to CAD tools, an ANN was used to predict crosstalk given data on the driver, the load and the length of the interconnect. See sections 2.2-4.1.

19. ***Petschauer et al. ('506)*** disclose "*Method of fabricating IC chips with equation estimated peak crosstalk voltages being less than noise margin.*" They further disclose that in one method according to the present invention, an integrated circuit chip is fabricated by the following steps:

1) providing a trial layout in the chip for a victim net and a set of aggressor nets which have segments that lie next to the victim net;

2) assigning to the trial layout of the victim net, the parameters of--a line capacitance, a line resistance, and a driver output resistance; and assigning to the trial layout of each aggressor net, the parameters of--a coupling capacitance to the victim net, and a voltage transition;

3) estimating, for each aggressor net, a respective peak crosstalk voltage V.sub.p which the aggressor net couples into the victim net as a function V.sub.p =K(e.sup.-X -e.sup.-Y) where K, X, and Y are products of said parameters;

4) modifying said trial layout and repeating the assigning and estimating steps until a summation of the estimated peak crosstalk voltages in the victim net is within an acceptable level; and,

5) building the chip with the modified layout for which the summation is

within the acceptable level.

See fig. 4-9, 25 and corresponding text.

20. **Li et al.** disclose that as process technology scales down to deep sub-micron and the frequency of a high-performance processor increases beyond 300 MHz, coupling induced signal integrity problems become more severe. Ignoring coupling effects can lead to functional failures or speed degradation. As a result, the traditional approach of **repeater** insertion driven by propagation **delay** and slew rate optimization becomes inadequate. The authors propose a design methodology to select optimal **repeaters** for high-performance processors by considering not only the **delay** and slew rate, but also **crosstalk** effects. A concurrent decision diagram (CDD) is further suggested to achieve **crosstalk** constraints with various trade-offs. See section IV (Proposed Methodology) including step 1 (Delay-ratio consideration); step 2 (Repeater-delay consideration); step 4 (With vs. witout repeaters: delay and skew); step 5 (Crosstalk consideration); step 6 (CDD alternatives and trade-offs). Particularly note fig. 3 (crosstalk voltage dependence on wire length); fig. 6 (design algorithm taking into consideration delay, crosstalk wire length, driver strength in an iterative constraint methodology); fig. 11 (delay dependence on presence of repeaters and as a function of wire length); fig. 13-14 (relationship between crosstalk and driver strength); fig. 15 (relationship between crosstalk, wire length and driver strength).

21. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of (Alpert et al. or Tawada or Jones et al. or Dwyer et al.) to take into consideration of the recited curves and/or to modify the drivers with the

secondary teachings for the following reasons: There are two techniques in this art to solve the crosstalk noise problem (which, by definition, inherently depends upon a criterion which defines acceptable vs. unacceptable noise) - 1) increase the driver strength and 2) insert buffers when the conductors are too long. Both were extremely well known in the art at the time of the invention. Applicants have admitted (first paragraph, page 2) that it was known to "*...increase the size of the driver supplying signals to a conductive path which is deemed to be noise sensitive.*". Applicants have also admitted (first full paragraph, page 5) that "*It is well known that a conductive path of a given length being driven by a weak driver will have a higher susceptibility to noise than that same conductive path when driven by a stronger driver.*" These features are also disclosed in Oh et al., Davis et al., Yang et al. and Petschauer et al., as noted earlier. If increasing the driver strength is not sufficient to solve the noise problem, then buffers would *also* be required to reduce the noise. Furthermore, If the placement of buffers is not sufficient to solve the noise problem, then increasing the strength of the drivers would *also* be required to reduce the noise.

22. Claims 15, 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over [Alpert et al. (6,117,182) or Tawada or Jones et al. or Dwyer et al.] in view of (Applicant's Own Admission) or Oh et al. or Davis et al. or Yang et al. or Petschauer et al. in further view of Li et al..

23. (Alpert et al. or Tawada or Jones et al. or Dwyer et al.) further do not expressly disclose taking into account delay issues caused by the insertion of the buffers/drivers/repeaters.

24. **Li et al.** disclose disclose taking into account delay caused by the insertion of buffers. Li et al. discloses that as process technology scales down to deep sub-micron and the frequency of a high-performance processor increases beyond 300 MHz, coupling induced signal integrity problems become more severe. Ignoring coupling effects can lead to functional failures or speed degradation. As a result, the traditional approach of **repeater** insertion driven by propagation **delay** and slew rate optimization becomes inadequate. The authors propose a design methodology to select optimal **repeaters** for high-performance processors by considering not only the **delay** and slew rate, but also **crosstalk** effects. A concurrent decision diagram (CDD) is further suggested to achieve **crosstalk** constraints with various trade-offs. See section IV (Proposed Methodology) including step 1 (Delay-ratio consideration); step 2 (Repeater-delay consideration); step 4 (With vs. witout repeaters: delay and skew); step 5 (Crosstalk consideration); step 6 (CDD alternatives and trade-offs). Particularly note fig. 3 (crosstalk voltage dependence on wire length); fig. 6 (design algorithm taking into consideration delay, crosstalk wire length, driver strength in an iterative constraint methodology); fig. 11 (delay dependence on presence of repeaters and as a function of wire length); fig. 13-14 (relationship between crosstalk and driver strength); fig. 15 (relationship between crosstalk, wire length and driver strength).

25. It would have been obvious to one of ordinary skill in the art at the time of the invention to take into account such issues for the followings reasons. Delays are inherently associated with buffers. It is therefore, inherent that insertion of a buffer on a wire will change the timing associated with the wire, as noted by Li et al. (see, for

example, section III – pg. 727; and "Step 4" – pg. 728). Li discloses taking such factors into account (see fig. 5, algorithm – especially step 5).

Response to Arguments - (paper # 17)

26. Applicant's arguments have been fully considered, but they are not persuasive.

Response to Arguments - Information Disclosure Statement

27. Applicants have been silent in response to paragraph 31 of paper # 8 and paragraph 19 of paper # 16. The Examiner notes that while the alleged deficiencies of prior art have been discussed in the specification (see section 2 ["the background art"] of the specification, for example), and Applicants have admitted that the concepts expressed in figures 1-2 are prior art, there has been no mention, in an IDS, of such prior art. The Examiner extends full faith and credit to Applicants, based on their repeated silence, that they are not aware of relevant prior art.

***Response to Arguments - 112 Rejections* (pp. 12-13, paper # 17)**

28. The 112 rejections relating to "choosing an insertion point so as to yield a "most acceptable integrated circuit timing characteristic" are withdrawn in view of the amendment (paper # 17).

***Response to Arguments - 102 Rejections* (pp. 15-16, paper # 9; pp. 13-16, paper # 17)**

29. Applicants arguments are not persuasive with respect to the Petschauer rejections. Applicants allege that Petschauer does not contain the recited limitation. Please see figures 4 and 25. - ***Petschauer et al. ('506)*** disclose "*Method of fabricating IC chips with equation estimated peak crosstalk voltages being less than noise margin.*" They further disclose that in one method according to the present invention, an integrated circuit chip is fabricated by the following steps:

1) providing a trial layout in the chip for a victim net and a set of aggressor nets which have segments that lie next to the victim net;

2) assigning to the trial layout of the victim net, the parameters of--a line capacitance, a line resistance, and a driver output resistance; and assigning to the trial layout of each aggressor net, the parameters of--a coupling capacitance to the victim net, and a voltage transition;

3) estimating, for each aggressor net, a respective peak crosstalk voltage V.sub.p which the aggressor net couples into the victim net as a function V.sub.p =K(e.sup.-X -e.sup.-Y) where K, X, and Y are products of said parameters;

4) modifying said trial layout and repeating the assigning and estimating steps until a summation of the estimated peak crosstalk voltages in the victim net is within an acceptable level; and,

5) building the chip with the modified layout for which the summation is within the acceptable level.

See fig. 4-9, 25 and corresponding text.

Response to Arguments - 103 Rejections (pp. 19-20, paper # 9; pp. 16-21, Paper # 17)

30. Applicant's arguments are not persuasive.

31. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

32. Applicant's arguments relating to Applicant's Own Admission is noted but not persuasive. **Applicants have admitted the following:**

- page 2 (first paragraph) is Applicant's Admission regarding prior art teaching of the relationship between drivers and noise and the use of different drivers to counteract the effects of noise;

- figures 1-2 (and second full paragraph, page 5, specification, relating to figure 2);

- page 3, last paragraph, page 9, last paragraph and page 10 are Applicant's admittance regarding the ability of a skilled artisan;

- page 5, (first full paragraph) is Applicant's Admission regarding prior art teaching of curves for various driver circuits of noise amplitude vs. length of lines;

- page 5, (first full paragraph) is Applicant's Admission regarding prior art teaching of the lower susceptibility of wires to noise for stronger drivers;

- page 6, (second paragraph - lines 1-4) is Applicant's Admission regarding prior art teaching of criterion for noise levels.

33. Applicant's argument that the combination of prior art does not teach the claimed invention is also not persuasive. The Examiner has argued:

> "There are two techniques in this art to solve the crosstalk noise problem (which, by definition, ***inherently*** depends upon a criterion which defines acceptable vs. unacceptable noise) - 1) increase the driver strength and 2) insert buffers when the conductors are too long. Both were extremely well known in the art at the time of the invention. Applicants have admitted (first paragraph, page 2) that it was known to "*...increase the size of the driver supplying signals to a conductive path which is deemed to be noise sensitive.*". Applicants have also admitted (first full paragraph, page 5) that "*It is well known that a conductive path of a given length being driven by a weak driver will have a higher susceptibility to noise than that same conductive path when driven by a stronger driver.*" These features are also disclosed in Oh et al., Davis et al., Yang et al. and Petschauer et al., as noted earlier. If increasing the driver strength is not sufficient to solve the noise problem, then buffers would *also* be required to reduce the noise. Furthermore, If the placement of buffers is not sufficient to solve the noise problem, then increasing the strength of the drivers would *also* be required to reduce the noise."

34. Applicants have not adequately addressed such argument and are therefore, not persuasive. Applicants have merely recited limitations and alleged that the limitations are not disclosed. Furthermore, *Applicants have not adequately addressed the specifics of the rejections, including the cited passages in the asserted prior art.*

Conclusion

35. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

36. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

37. Any inquiry concerning this communication or earlier communications from the examiner should be:

directed to:

Dr. Hugh Jones telephone number (703) 305-0023, Monday-Thursday 0830 to 0700 ET, ***or*** the examiner's supervisor, Kevin Teska, telephone number (703) 305-9704. Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist, telephone number (703) 305-3900.

mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 308-9051 (for formal communications intended for entry)

or (703) 308-1396 (for informal or draft communications, please label "*PROPOSED*" or "*DRAFT*").

Dr. Hugh Jones

Primary Patent Examiner

January 3, 2004

HUGH JONES Ph.D
PRIMARY PATENT EXAMINER
TECHNOLOGY CENTER 2100